Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-21 are pending in the application, with claims 1, 8, 18-20 being the independent claims. New claims 15-21 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Prior Art Rejections

In the first Office Action dated March 18, 2002, claims 1, 3-8 and 10-14 were rejected under 35 U.S.C. § 102 (e) as allegedly being anticipated by U.S. Patent No. 6,096,610 to Alavi et al. (hereinafter Alavi '610 or just "Alavi"). Claims 2 and 9 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Alavi. The Examiner reasserted all of these claim rejections in the final Office Action dated September 17, 2002. Applicants respectfully traverse.

Claims 1 and 8

Claims 1 and 8 are amended to include the inventive feature that the write transistors have "thicker" oxide layers than does the programmable capacitor. This "thicker" oxide

layer feature is also recited in claims 5 and 12, and new claim 21. Specifically, each of amended claims 1 and 8 recites in part:

> a write switch including plural transistors each having a gate oxide layer that is *thicker* than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer. (Emphasis added.)

The present invention recited in claims 1 and 8 (and 5 and 12) avoids the problem of junction breakdown during programming because of the thicker oxide layers of the write switch transistors compared to that of the capacitor. Specifically, the thicker oxides layers of the write switch transistors enable these transistors to tolerate the voltage required to program the capacitor. Alavi does not disclose or suggest the feature of the "thicker" oxide layer recited in claims 1 and 8 (and 5 and 12).

Discussion of Alavi

Alavi is directed to program circuits used to program a fuse. Alavi discusses problems associated with program transistors made with the *same* process as a fuse having a 3.5 nanometer oxide thickness and a corresponding oxide breakdown voltage of 5.5 volts. Alavi, C4, L13-31. Use of the *same* process suggests that the program transistors have the *same* oxide thickness as the fuse, not a *thicker* oxide thickness. As a result, the program transistors can not withstand the "at least 7 volts" required to burn the fuse. That is, the program transistors suffer undesirable junction breakdown at the program voltage.

To avoid undesired junction breakdown, Alavi discloses two solutions. First, Alavi proposes "special" high voltage transistors. For example, circuits 30 (FIG. 2A) and 40 (FIG.

2B) include "special" high voltage transistors 34 and 44, respectively, which are tolerant to a program voltage of 8 volts. C4, L34 – C5, L62; C4, L14-17 and C5, L47. Also, circuits 201 (FIGs. 2C and 2D) for programming a fuse 207, include "special" high voltage transistors 219 and 265. C7, L21-27 and L58-63.

With reference to FIG. 4, Alavi describes an example construction of a "special" high voltage transistor 433. C10, L66-C12, L9; C11, L49-58; C12, L7-10. The "special" transistor construction of FIG. 4 uses carefully selected semiconductor doping concentrations for different transistor regions to achieve its required high voltage tolerance. C11, L38-56 and L64-67. Nowhere does Alavi mention or suggest that the "special" transistor has an oxide layer that is "thicker" than that of the fuse to be programmed, as is recited in claims 1 and 8 (and 5 and 12).

Another approach to avoid junction breakdown used in Alavi is a program circuit configuration that avoids exposing support transistors to the full programming voltage (8 volts). For example, see C5, L6-10 and L59-62; C7, L3-6; and C8, L1-8. In such an arrangement, the support transistors need not be tolerant to the full 8 volts used to program the fuse.

Thus, Alavi teaches mechanisms to avoid junction breakdown *other than* a gate oxide layer that is *thicker than* said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor, as is recited in amended claims 1 and 8. Applicants have reviewed Alavi carefully and can not find therein any disclosure or suggestion of the "thicker" oxide layer feature.

Amended claims 1 and 8, claims 5 and 12, and claim 21 are believed patentable for at least all of the reasons advanced above. Also, all of the claims depending from claims 1

and 8 are believed patentable for at least the same reasons claims 1 and 8 are patentable.

Claims 2, 9 and 18

Claims 2, 9 and new claim 18 each recite the feature that the oxide layer thickness is approximately 20 Angstroms. On page 4 of the first Office Action, the Examiner rejected claims 2 and 9 under 35 U.S.C.§ 103(a) as allegedly being unpatentable over Alavi. The Examiner alleges it would have been obvious to use a 20 Angstrom thick oxide layer as recited in claims 2 and 9 since it has been held that discovering an optimum value of a result-effective variable involves only routine skill in the art. The Examiner further asserts that one of ordinary skill would have been motivated to form the claimed 20 Angstrom thick oxide layer for at least the purpose of providing an anti-fuse layer. Applicants respectfully disagree for at least the following reasons.

Before the determination of the optimum range of a parameter/variable (i.e., the fuse oxide layer thickness) might be characterized as routine, the parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result. MPEP 2144.05 II.B; *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977). Alavi fails to recognize that the oxide layer thickness is result-effective. Thus, Alavi can not be said to motivate one of ordinary skill to use the claimed 20 Angstrom oxide layer thickness.

In contrast, Applicants recognized that the oxide layer thickness is a result-effective variable. Applicants recognized that an oxide layer thickness of approximately 20 Angstroms has advantageous properties. For example, the 20 Angstrom thick oxide layer facilitates a controlled rupture during programming due to a tunneling effect recited in

claims 1 and 8. Advantageously, this controlled rupture minimizes a spread in the resistance of programmed fuses, which results in a simplified sense or read circuit compared to the prior art. These properties and advantages of the present invention are discussed in the present application, for example, at page 5, L9-14; page 6, L3-13; and page 8, L26-28; page 9, L24-page 10, L2. An even further property of the 20 Angstrom thick oxide layer is the commensurately lowered programming voltage required to rupture the oxide layer.

In contrast, Alavi teaches a 35 Angstrom oxide layer thickness, which results in a fuse rupture that leads to an undesirable spread in programmed fuse resistance. As a result, Alavi is forced to resort to a specially adapted or "carefully optimized" sensing transistor 225, that is:

> sized small enough to provide reasonable sensing margin *which makes it insensitive to any fluctuation in the resistance of a fused antifuse device 207*, but large enough . . . for reasonable sensing. (Italics added)

Alavi C8, L30-33.

It follows that Alavi fails to recognize that an oxide layer reduced from 35 Angstroms to 20 Angstroms in thickness, as is claimed, (i) facilitates controlled oxide layer rupture, (ii) reduces the undesired "fluctuation in the resistance of a fused antifuse device," and (iii) thereby may avoid the need in Alavi for the "carefully optimized" sensing transistor. Thus, Alavi fails to recognize that the oxide layer thickness is a result-effective variable. Accordingly, Alavi teaches only a 35 Angstrom oxide layer thickness, and does not suggest an approximately 20 Angstrom thick oxide layer thickness, as is recited in claims 2, 9 and 18.

Claims 2, 9 and 18 are believed patentable for at least all of the reasons advanced above.

The 20 Angstrom thick oxide layer has the advantage that it may be ruptured with a lower program voltage than that used to rupture the 35 Angstrom thick oxide layer of Alavi. For example, the present invention uses a program voltage of less than 7 volts (e.g., 5 volts) as is claimed in amended claims 5, 12 and new claim 17. In contrast, Alavi teaches that the program voltage needs to be "at least 7 volts." Alavi C4, L21-24. In fact, Alavi uses a program voltage of 8 volts throughout. Claim 5, 12, and new claim 17 are also patentable for at least this reason.

Claims 4 and 19

Amended claim 4 and new claim 19 recite the feature of a deep N-well design of the programmable capacitor/transistor. The deep N-well design is further defined as including:

> a P-well layer adjacent the source and drain regions;
> a deep N-well layer below the P-well layer; and
> a P-type substrate below the deep N-well layer.

These features are not disclosed or suggested in Alavi.

On page 3 of the first Office Action, the Examiner asserted that Alavi teaches claims 4 and 11, citing to a transistor component (405) of FIG. 4 of Alavi. Applicants respectfully point out to the Examiner that FIG. 4 of Alavi is directed to the "special" high voltage transistor used to program fuse 207, *not* to the fuse itself. Therefore, FIG. 4 in Alavi is not relevant to the features of the programmable capacitor recited in the claims of the present invention.

Amended claim 4, claim 11 and new claim 19 are all believed to be patentable for at least the reasons advance above.

Claims 5, 12 and 17

Amended claims 5 and 12, and new claim 17, recite that the programming voltage applied across the capacitor oxide layer is less than 7 volts. In contrast, Alavi states "at least 7 volts" is required to program the fuse, as discussed above. In fact, Alavi uses 8 volts throughout. Thus, Alavi neither discloses nor suggests this feature. In fact, Alavi teaches away from this feature. Therefore, claims 5, 12 and 17 are believed patentable over Alavi.

Claim 16

New claim 16 recites the feature of a *read* transistor having an oxide layer that is *thicker than* the oxide layer of the programmable capacitor. This feature is not disclosed or suggested in Alavi.

Claim 18

New claim 18 combines the features of original claims 1 and 2, less the feature of "direct gate tunneling current" recited in original claim 1.

Claim 19

New claim 19 combines the features of original claim 1 (less the "direct gate tunneling current" feature), original claim 3, and amended claim 4.

Claim 20

New claim 20 recites an inventive configuration of a write circuit used to program a capacitor. An example of the claimed write circuit is depicted in FIG. 2 of the present application.

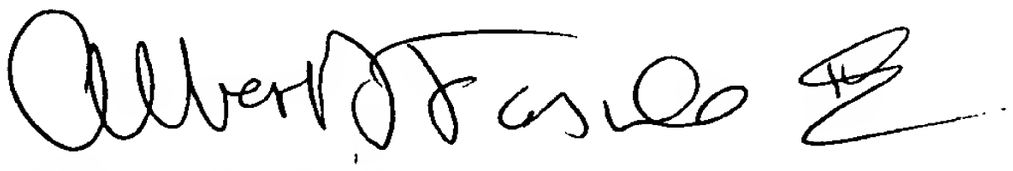
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Albert J. Fasulo, II
Attorney for Applicants
Registration No. 43,607

Date: April 11, 2003

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

::ODMA\MHODMA\SKGF_DC1;119293;1

Version with markings to show changes made

1. A one-time programming [programing] memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current; and

a write switch [having] including plural transistors each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer;

wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said capacitor oxide layer via said [switch] write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

2. The one-time programming [programing] memory element according to claim 1, wherein said capacitor oxide layer is approximately 20Å thick.

3. The one-time programming [programing] memory element according to claim 1, wherein said capacitor comprises a field effect transistor having source and drain regions coupled to ground, a gate coupled to said switch and a gate dielectric forming said oxide layer.

4. The one-time programming [programing] memory element according to claim 3, wherein said field effect transistor has a deep N-well design including:

a P-well layer adjacent the source and drain regions;

a deep N-well layer below the P-well layer; and

a P-type substrate below the deep N-well layer.

5. The one-time programming [programing] memory element according to claim 1, wherein said write switch comprises a 5 volt tolerant switch having plural 2.5 volt transistors with gate oxide layers that are thicker than said capacitor oxide layer, and wherein said voltage is less than 7 volts.

6. The one-time programming [programing] memory element according to claim 1, further comprising a sensing circuit to sense whether said capacitor is programmed.

7. The one-time programming [programing] memory element according to claim 1, wherein a charge pump is not required to program said anti-fuse.

8. A process, compatible with 0.13μm or below CMOS technology, for making a one-time programming [programing] memory element, comprising the steps of:

forming a capacitor having an oxide layer capable of passing direct gate tunneling current; and

forming a write switch [having] including plural transistors each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer;

wherein said capacitor is one-time programmable as an anti-fuse, without a charge pump, by application of a voltage across said capacitor oxide layer via said switch to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

9. The process according to claim 8, wherein said capacitor oxide layer is formed to a thickness of approximately 20Å thick.

12. The process according to claim 8, wherein said forming switch step comprises forming a 5 volt tolerance switch having plural 2.5 volt transistors with gate oxide layers that are thicker than said capacitor oxide layer, and wherein said voltage is less than 7 volts.

New claims 15-21 have been added.